A 10 MHz OCVCXO and PLL Module

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Introduction

This paper describes a PLL and interface module for the HP 10811A oven-controlled voltage-controlled crystal oscillator (OCVCXO). It comprises supporting mechanical, power and monitoring circuitry for the oscillator unit, dual RF output buffer amplifiers, and means for tuning or phase locking it to an external 10 MHz reference. The module can be implemented either as a bare board (Figure 1) or packaged in an instrument case (Figures 2 and 3). The front panel controls comprise an open loop (OL) frequency adjustment potentiometer, an OL/PLL mode switch, an analog meter showing the phase detector voltage, two 10 MHz RF outputs, and LED indicators for oven demand and applied power. The rear panel has 10 MHz reference and +24 VDC inputs.

Figure 1. OCVCXO and PLL Interface Board

Figure 2. Front Panel

Figure 3. Rear Panel

The 10 MHz OCVCXO and PLL Module Housed in a Hammond 1426K Instrument Case

An RCA jack was subsequently added to the rear panel to bring out the OCVCXO control voltage via a 1 kΩ and 0.1 µF low pass filter.

Description

A block diagram of the OCVCXO and PLL module is shown in Figure 2. The HP10811A interface board supports operation either free-running or phase locked to an external 10 MHz reference. It provides two buffered 10 MHz outputs and operates from a single +20 to +24 VDC supply which directly powers the crystal oven, is regulated at +12 volts for the oscillator, and converted to ±5 volts for the RF and PLL circuits. Buffer amplifier isolate the two phase detector inputs. In the open loop mode, the frequency may be adjusted via a tuning potentiometer and its beat observed on an analog meter against an external reference. In the PLL mode, the oscillator is phase locked to the external reference. Monitor LEDs show the crystal oven and internal +12 volt power status.

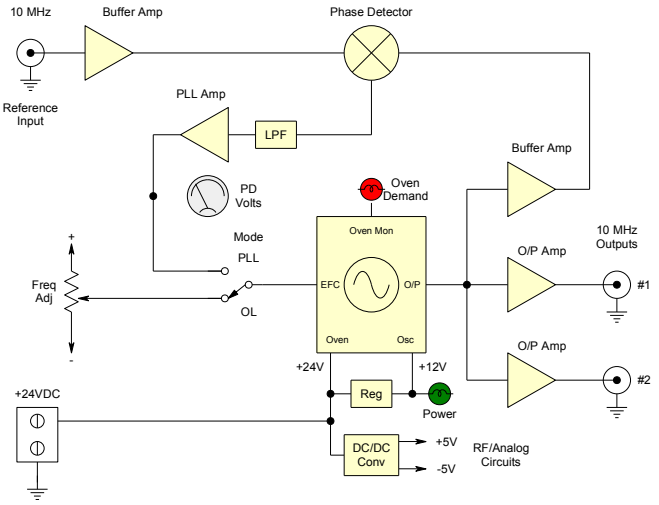

Figure 4. Block Diagram of OCVCXO and PLL

Circuit

Schematics of the 10 MHz OCVCXO and PLL and interface module are shown in Figures 5-8. The OCVCXO section interfaces the oscillator with its power supplies, electronic tuning and oven monitor. The RF amplifier section has three unity gain +7 dBm nominal 50 Ω input/output amplifier circuits to provide two 10 MHz outputs and drive to the phase detector RF port. The PLL section accepts a buffered +7 dBm nominal 50 Ω 10 MHz external reference to the phase detector reference input. The double-balanced mixer (DBM) type analog phase detector is followed by a low pass filter and DC amplifier to produce a control voltage for the OCVCXO. The power section comprises a low noise +12 volt regulator and a well-filtered ±5 volt DC/DC converter.

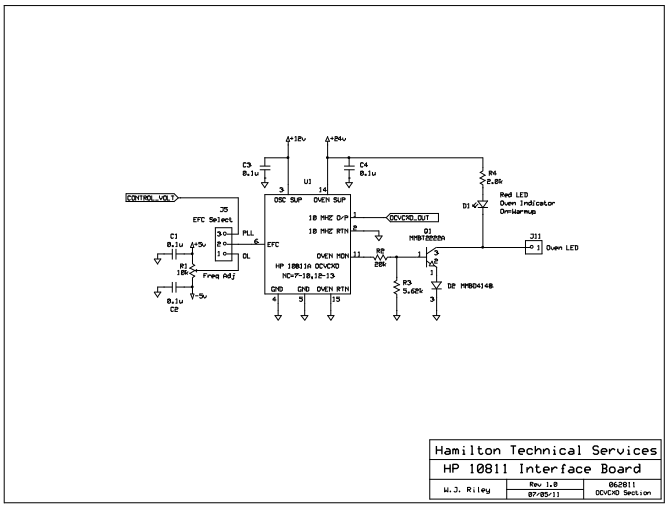

Figure 5. OCVCXO Section

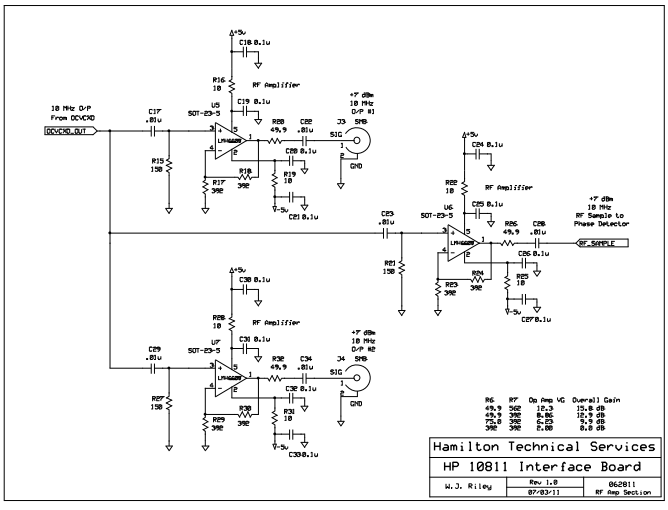

Figure 6. RF Amplifier Section

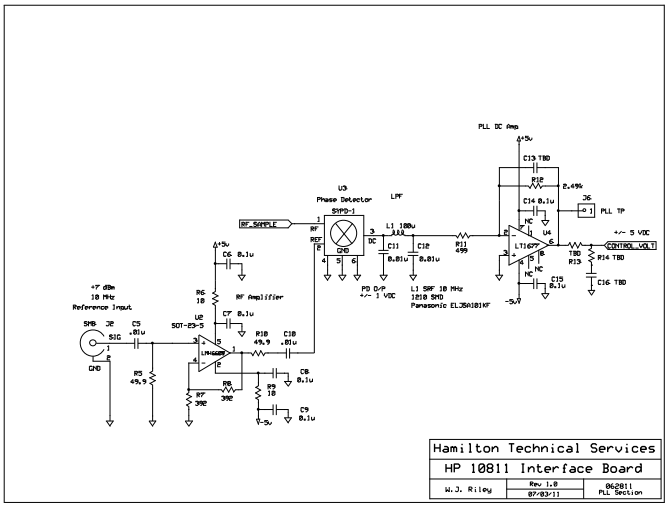

Figure 7. PLL Section

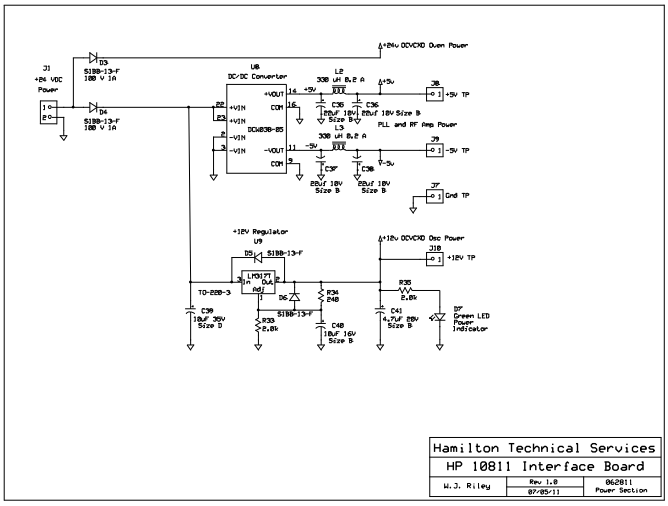

Figure 8. Power Section

Board Layout

The 3.8" x 2.5" circuit board layout of the 10 MHz OCVCXO and PLL and interface module is shown in Figures 9 and 10. The HP10811A oscillator plugs into a 15-pin double row PWB connector. The passive components are mainly 0603 SMD parts. External DC power is applied to a terminal strip, RF inputs and outputs are via SMB jacks, and 0.1" headers provide various external control and monitor connections.

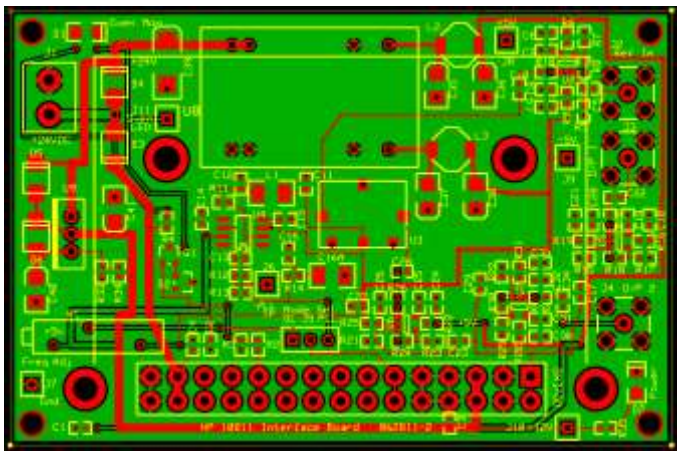

Figure 9. PWB Layout

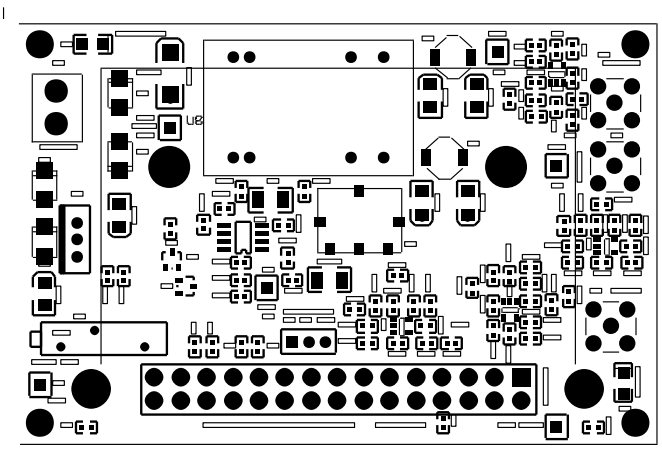

Figure 10. PWB Silk Screen

A photograph of the assembled board without the oscillator is shown in Figure 11. It comprises a single 3.8" x 2.5" board into which the OCVCXO plugs with a 15-pin edge connector. The large black component is the DC/DC converter and the smaller white object at the center of the board is the phase detector.

The 12 volt TO-220 reguator has enough dissipation (around 0.3 watt) that heat sinking is desirable. The original concept was to sink it to the OCVCXO case, but that case gets nearly as hot as the bare regulator. Thus the final arrangement uses a convective heat sink atttached to the regulator with a nylon spacer attached to the OCVCXO that provides mechanical support. The mounting screw is electrically isolated by fiber shoulder washers in the heat sink and regulator. No mechanical support is needed for the heat

sink if the module is packaged inside an instrument case. The measured temperatures were +46°C and +42°C respectively at the heatsink and OCVCXO top with the bare module in +28°C still air.

The measured ripple on the +12 volt, +5 volt and -5 volt power supplies was below 1 mV p-p. The measurement was limited by the grounding and general laboratory EMI, and there was no obvious dominant spectral component.

Figure 11. Assembled OCVCXO and PLL Board

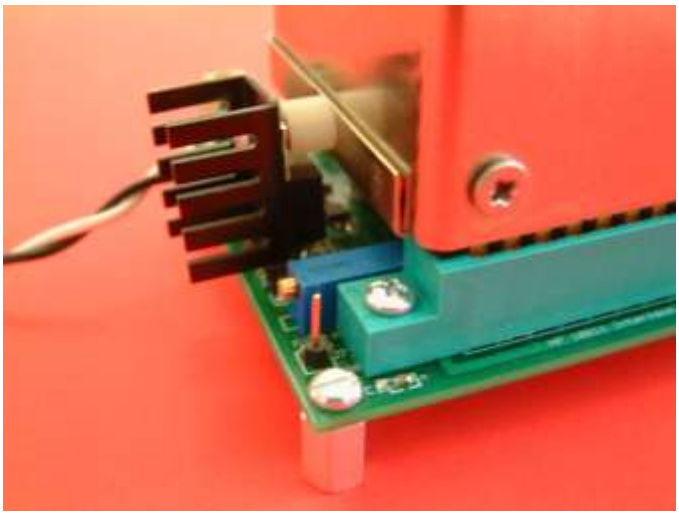

Figure 12. 12 Volt Regulator Heat Sink

Board Configuration

The OCVCXO and PLL board can be used in either a stand-alone configuration or housed in an instrument case. The external connections for the latter are shown in Figure 13. These allow the board be connected to external controls and indicators for use in an instrument box. The unit can to be operated either open loop as a voltage tuned oscillator or closed loop with the oscillator phase locked to an external reference. The open loop (OL) tuning voltage can be read from a digital dial on the tuning potentiometer, and the phase detector output observed on an analog panel meter. In the stand-alone configuration, an on-board tuning potentionmeter is provided, and an OL/PLL mode switch can be installed on the bottom of the board as shown in Figure 14.

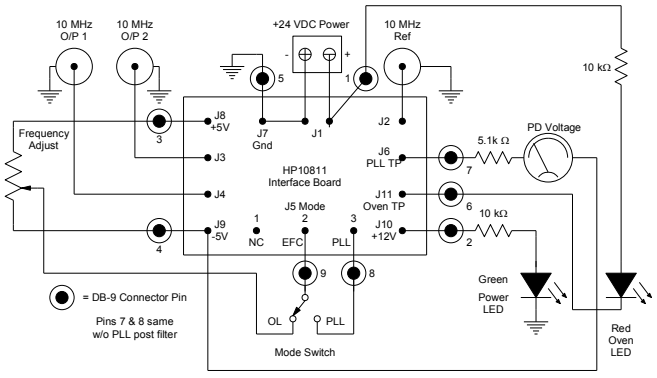

Figure 13. External Connections

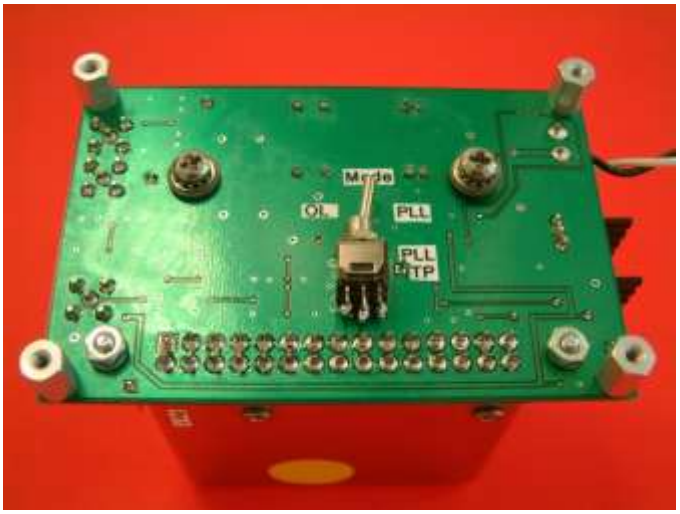

Figure 14. Mode Switch

OCVCXO Tuning Characteristic

The electronic frequency control (EFC) characteristic of HP10811-60111 S/N A06116 is shown in Figure 16. This plot shows the EFC tuning characteristic of HP 10811-60111 over its specified range from -5 volts to +5 volts which provides a tuning range of about 2.0×10^{-7} that can be centered with the OCVCXO coarse mechanical frequency adjustment. The measured average tuning slope is about -0.2 Hz/volt or -2×10^{-8}/volt. The characteristic is reasonably linear over the entire range.

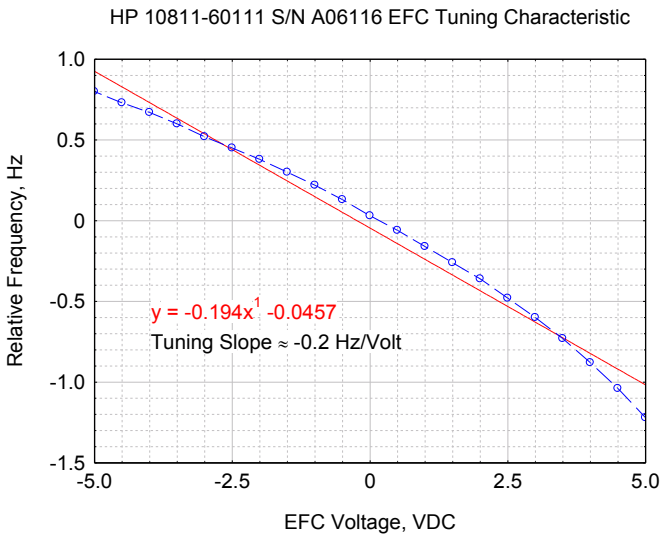

Figure 16. EFC Tuning Characteristic

PLL Transient Response

The transient response of HP10811A PLL was measured by applying a 12 voltage step to the inverting input of the loop DC amplifier via a 24 kΩ resistor and the response was observed at its output as shown in Figure 16. The oscilloscope trace scales are 200 mV/div vertical and 50 ms/div horizontal. The PLL time constant is about 0.2 second and the loop bandwidth is about 0.8 Hz. The response is the damped exponential of a 1st order PLL which can acquire lock without any additional circuitry provided only that the oscillator's tuning range reaches the reference frequency.

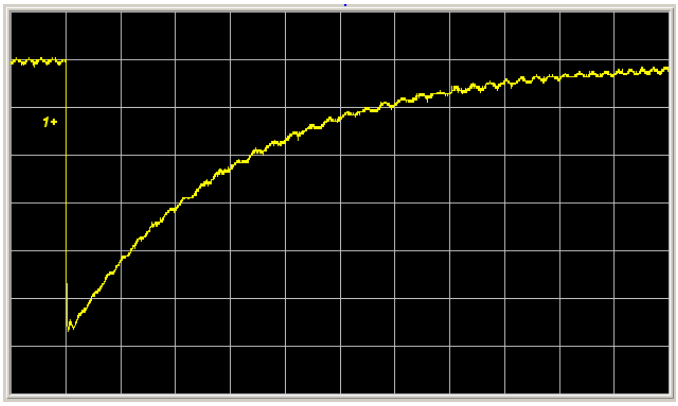

Figure 16. PLL Transient Response

The HP10811A PLL is, for all practical purposes, a 1st order phase locked loop. The additional high frequency break of the PLL DC amplifier is at 640 Hz, far above the open loop bandwidth. There is, of course, no PLL divider, so the loop bandwidth, f_c, can be estimated as the product of the phase detector, amplifier and varactor gains, k_φ=0.5 V/rad, k_a=5 and k_v=0.2 Hz/V. This yields f_c=0.5 Hz, in reasonable agreement with the estimate based on the measured loop transient response.

The PLL response can be made faster (e.g., from a 200 ms to a 40 ms time constant) by increasing the loop amplifier gain (e.g., from about x5 to x24) by increasing the value of R12 (from 2.49 kΩ to 12.1 kΩ), which makes the unit more suitable for making tight PLL frequency measurements.

There is no practical means of lock detection for this slow analog PLL other than manual observation of the phase detector voltage.

Phase Noise

The output phase noise of the OCVCXO and PLL module will be equal to that of the OCVCXO itself for all sideband frequencies above about 1 Hz, as shown in the table of Figure 17 for a generic HP10811A/B oscillator at 10 MHz.

Sideband Frequency Hz	Phase Noise dBc/Hz
1	-90
10	-120
100	-140
1k	-145
10k	-150

Figure 17. Specified OCVCXO Phase Noise

Instrument Packaging

An interior view of the packaged unit is shown in Figure 18. The HP10811A OCVCXO and PLL interface board is mounted to the bottom of the case, and is connected to the front and rear panel RF connectors by three custom SMB plug to BNC jack cables. The analog panel meter shows the phase detector voltage, which is zero without an external reference, shows the open loop beat note with a reference, and shows the control voltage in the PLL mode, which can be centered by adjusting the oscillator coarse tuning. The front, rear and main assemblies are connectorized and can therefore easily be separated.

Figure 18. Interior View of OCVCXO and PLL

Instrument Open Loop Tuning Characteristic

The OCVCXO instrument open loop tuning characteristic was calibrated using a Thunderbolt GPS disciplined oscillator and a Brilliant Instruments BI220 time interval analyzer as a high resolution frequency counter. This calibration depends, of course, on the individual oscillator's coarse frequency adjustment, and will change with time due to oscillator aging. The frequency range is about -130 to +80 pp10^9 with zero-beat near the center of the dial, and it increases about 2.1×10^{-10} per dial division. The tuning characteristic can be closely fit to a quadratic function.

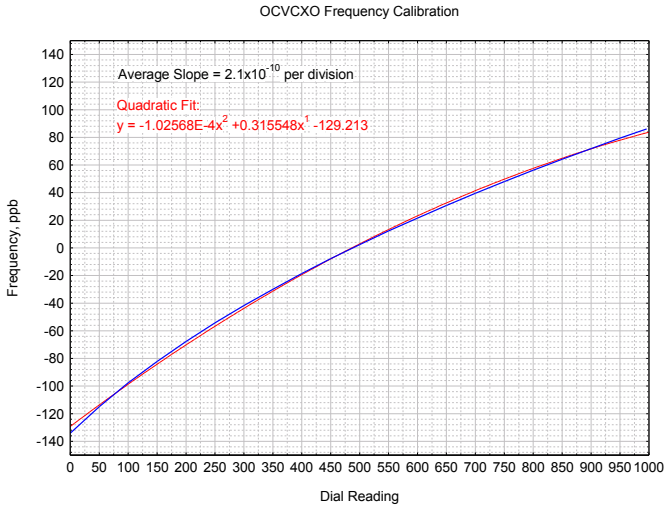

Figure 18. Instrument Tuning Characteristic

Open Loop Phase Detector Beat Note

The open loop phase detector beat note is a nominal ±5 volt peak-to-peak truncated triangular wave at the J6 PLL Test Point as shown in Figure 19.

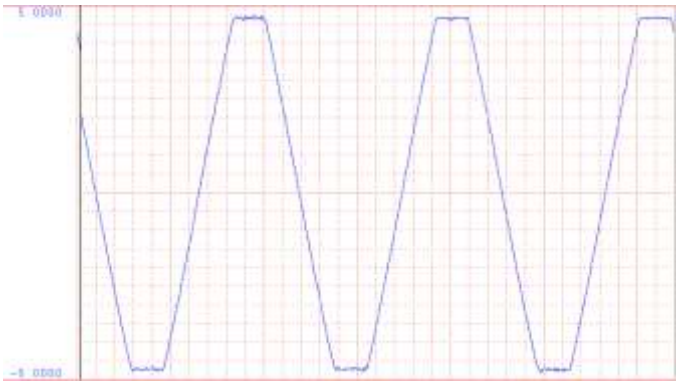

Figure 19. Open Loop Beat Note Waveform

Input and Output Return Loss

The measured reference input return loss was 34 dB at 10 MHz as shown in Figure 20. The measured RF output #1 return loss was 45 dB at 10 MHz as shown in Figure 21. The output #2 return loss characteristic was essentially identical, 43 dB at 10 MHz. The reverse isolation from output #1 to output #2 was 72 dB at 10 MHz and decreased smoothly to about -55 dB at 100 MHz. It was essentiallly the same between output #2 to output #1.

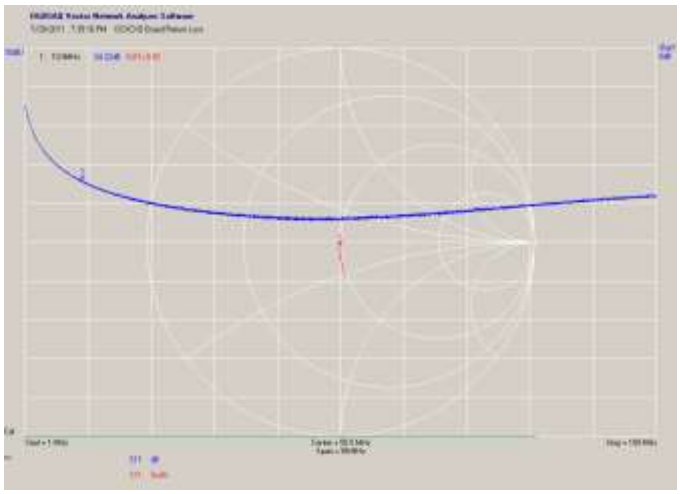

Figure 20. RF Input Return Loss vs Frequency

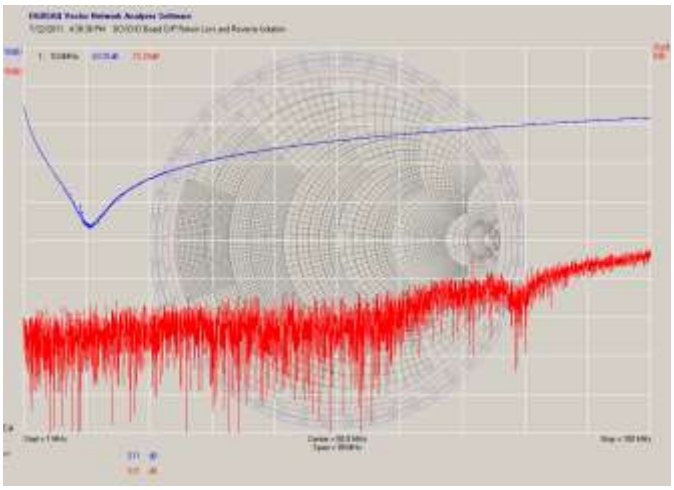

Figure 21. RF Output Return Loss vs Frequency

Spectral Purity

The output spectrum is clean within the resolution of the spectrum analyzer as shown in Figure 22. No spurious components are visible with any frequency span. The output harmonics are all ≥ 40 dB down as shown in Figure 23. The output power from both RF ouitputs was measured as +8.2 dBm.

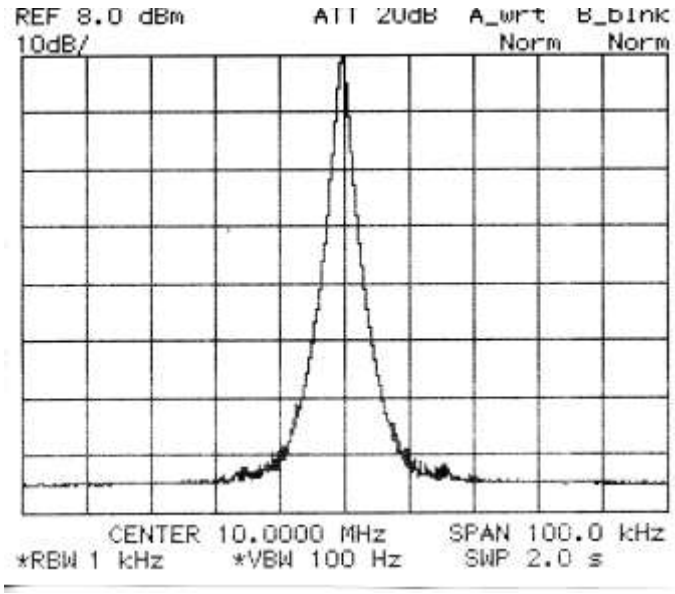

Figure 22. Carrier Spectral Purity

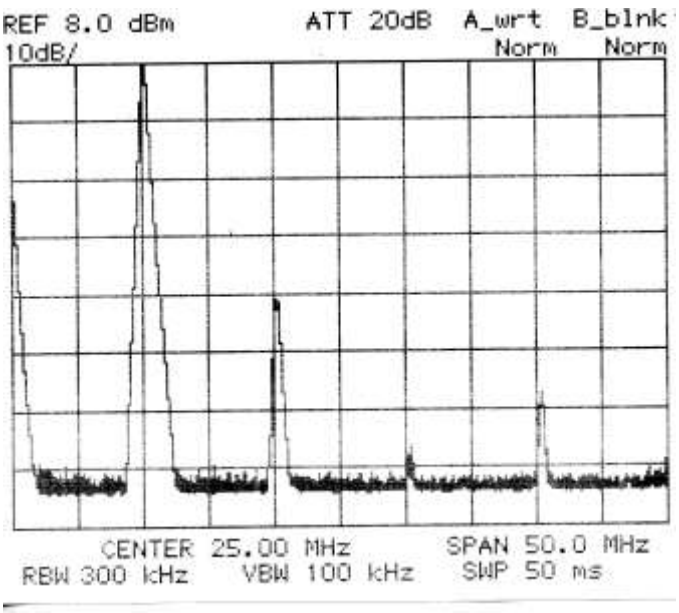

Figure 23. Harmonic Spectrum

- **Power Supply**

The recommended power supply for the 10 MHz OCVCXO and PLL module is a MeanWell GS25U24-P1J 24 volt, 1 ampere wall mounted type with a 2.1mm x 5.5 mm DC connector.

- **Operation**

The red oven demand and green power LEDs will illuminate when +24 VDC power is applied to the unit, and the former will turn off after the oven has reached control (several minutes for a cold start). Two isolated +7 dBm nominal 10 MHz RF outputs are provided.

Open loop operation is enabled by placing the mode switch in the OL position. The OCVCXO frequency can be adjusted with the tuning potentiometer which has a sensitivity of about 2.1×10^{-10} per dial division for the packaged instrument. The phase detector voltmeter will show the beat note between the free running OCVCXO and the external 10 MHz reference, but it is recommended that no external reference be applied for best spectral purity and stability.

Closed loop operation is enabled by placing the mode switch in the PLL position and applying an external 10 MHz reference. The phase detector voltmeter will show the OCVCXO control voltage, which can be centered by adjusing its coarse frequency trimmer at the top of the oscillator.

- **Applications**

Applications for this instrument in open loop mode include its use as a test source having good stability, low phase noise and excellent spectral purity. Its adjustable frequency with a known sense and calibrated magnitude that can verify the scale factor of a frequency measuring system. The module can serve as a phase-lockable frequency source for an instrument such as a counter, RF spectrum analyzer or synthesizer. Applications in closed loop mode include its use as a cleanup loop following a DDS synthesizer, and as a tight PLL frequency measuring system by observing and recording the calibrated OCVCXO control voltage.

An example of using this PLL module as a frequency measuring system is shown in Figure 24. HP 10811 ovenized crystal oscillators are used as both the locked oscillator and PLL reference, and the system thus shows the combined instability of two presumed identical and uncorrelated devices. The data are obtained by recording the band-limited PLL control voltage at a 10/second sampling rate with a 12-bit Dataq DI-158UP data acquisition system; the scale factor is $2x10^{-8}$ per volt with $1.2x10^{-12}$ resolution and is averaged by a factor of ten to τ = 1s. The resulting time-domain stability plot is corrected for one oscillator. The short-term noise for 1-100 seconds is flicker FM at about $1.0x10^{-12}$ which changes toward random walk FM and aging at longer averaging times with some visible room temperature A/C cycling.

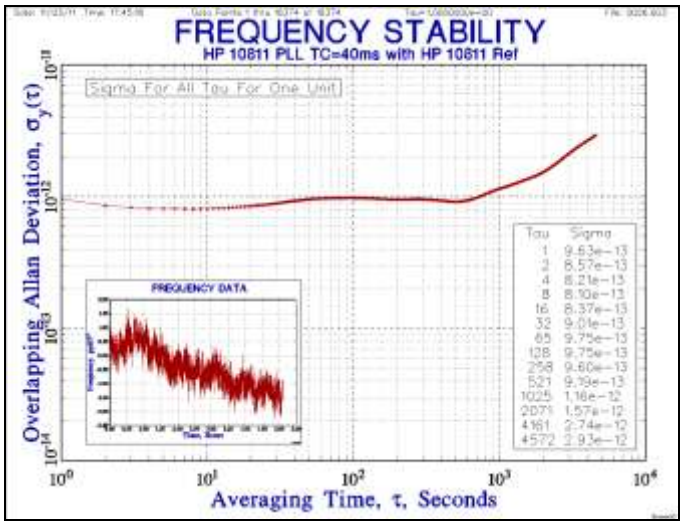

Figure 24. Stability Plot for a Single HP 10811 OCVCXO Using the PLL Module

An example of the use of the OCVCXO and PLL module as a clean-up filter for a rubidium frequency standard (RFS) is shown in Figure 25. The magenta (upper) curve shows the phase noise of an LPRO-101 rubidium measured against an HP 10811 OCVCXO. The 1 Hz phase noise corresponds to a combined 1-second short-term stability slightly better than $1x10^{-11}$, as expected for the RFS. The spectrum shows fairly strong spurs at 150 and 300 Hz caused by the RFS internal servo modulation as well as several other weaker ones at higher sideband frequencies. The noise floor is about -155 dBc/Hz. The blue (lower) curve shows the phase noise of the same source and reference but with the Rb signal filtered by the OCVCXO and PLL module. Notice that the loop acts as a low-pass filter, preserving the 1 Hz phase noise while eliminating the spurs and lowering the noise floor.

Figure 25. RFS Phase Noise With and Without OCVCXO and PLL Clean-up Filter

Specifications

Preliminary specification for the 10 MHz OCVCXO and PLL module are as follows:

Parameter	Specification	Remarks
10 MHz Reference Input Power	+7 dBm nominal sinewave into 50 Ω	This is enough to saturate the phase detector. A lower input level will decrease the PD phase slope.
10 MHz Reference Input Impedance	50 Ω ±5%	Return Loss ≥ 26 dB.
10 MHz OCVCXO Output Power	+7 dBm nominal sinewave into 50 Ω	Both outputs.
10 MHz Reference Input Frequency Range	$\pm 1 \times 10^{-7}$	For phase locking. Equal to OCVCXO EFC range. Center with coarse frequency adjustment,
10 MHz OCVCXO EFC Tuning Range	Same as above. Tuning slope ≈ 0.2 Hz/volt.	Open loop. Instrument tuning dial sensitivity ≈ 2×10^{-10}/division.
10 MHz OCVCXO output impedance	50 Ω ±5%	Return Loss ≥26 dB.
Output Inter-channel Isolation	≥60 dB	Between two outputs at 10 MHz.
Phase Noise	See Figure 17.	For generic HP 10811.
Short Term Stability (ADEV)	$\sigma_y(\tau=1\sigma) \leq 1 \times 10^{-11}$. See Reference 1 HP10811A specifications for other averaging times.	Open loop. Closed loop stability determined by reference for $\tau \geq 1$s.
Aging	$\leq 5 \times 10^{-10}$/day typical	For stabilized unit.
G Sensitivity	$\leq 2 \times 10^{-9}$ per g	For static tipover (2g)
Spurii	All ≤ -70 dBc	Non-harmonics.
Temperature Coefficient	$\leq 2.5 \times 10^{-9}$ over 0 to +70 °C	See Reference 1.
Parameter	**Specification**	**Remarks**
Harmonics	All ≤ -40 dBc	
PLL	Bandwidth ≈ 0.5 Hz. Time constant ≈ 0.2 seconds.	Automatic lock-up. Response can be made faster with larger R12.
DC Power	+24 VDC nominal at 0.6 ADC maximum warm-up demand. 0.3 A typical steady-state at room temperature (+25°C). Input voltage range +20 to +28 VDC.	Typical warm-up time < 5 minutes.
Size (HxWxD)	4" x 6" x 5"	Instrument configuration.
Weight	4.4 lbs. (1200 grams)	
Availability	Not for sale	Design information available at no cost upon request.

Reference

1. Hewlett-Packard, *10811A/B Quartz Crystal Oscillator Operating & Service Manual (V2)*, Manual Part Number: 10811-90002, August 1980.

File: A 10 MHz OCVCXO and PLL Module.doc
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